presently amends Claim 21 and 28, cancels Claims 22, 23 and 26 without prejudice or disclaimer. Accordingly, Claims 21, 24, 25 and 27-28 are currently pending in the application.

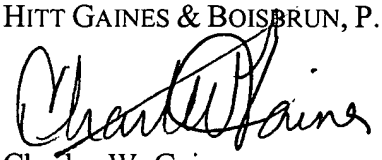
The Applicant believes that the presently amended claims are patentable over the references cited by the Examiner. Accordingly, the Applicant respectfully submits that the foregoing claims, as amended, are allowable. Therefore, a Notice of Allowance for Claims 21, 24, 25 and 27-28 is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Should it facilitate allowance of the application, the Examiner is invited to telephone the undersigned attorney. The Commissioner is hereby authorized to charge any additional payment that may be due or credit any overpayment to Deposit Account No. 08-2395.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



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PATENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Please amend Claim 21 as follows:

21. (Twice Amended) A semiconductor device, comprising:

a first metal feature located over a semiconductor surface and having a first etch stop layer and a first interlevel dielectric layer located thereover and a second etch stop layer and a second interlevel dielectric layer located over the first etch stop layer and the first interlevel dielectric layer[, the second interlevel dielectric layer having a second metal feature located in a surface thereof]; [and]

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the via extending [between] to and [connecting] contacting the first metal feature [and the second metal feature], the via being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion

extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

(2) Please cancel Claims 22, 23 and 26 without prejudice or disclaimer.

(3) Please amend Claim 28 as follows:

28. (Amended) The semiconductor device as recited in Claim 27 further including a second via that extends through the third dielectric layer and contacts the landing pad.